In re Patent Application of:
LENOBLE
Serial No. **10/714,440**
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In the Claims:

Claims 1-24 (Cancelled).

25. (Currently Amended) A process for fabricating an integrated circuit comprising:

forming a gate on a silicon substrate;

implanting dopants in the silicon substrate to form drain and source extensions therein;

amorphizing regions of the silicon substrate to obtain amorphous silicon regions adjacent the gate after implanting the dopants; and

~~implanting dopants in the amorphous silicon regions to form drain and source extensions therein; and~~

forming drain and source regions in the respective drain and source extensions with a channel being defined therebetween, the drain and source regions being formed at a temperature below 800°C.

26. (Previously Presented) A process according to Claim 25, wherein the silicon substrate comprises a crystalline silicon substrate.

27. (Previously Presented) A process according to Claim 25, further comprising forming spacers on the silicon substrate adjacent the gate after forming the drain and source extensions.

28. (Previously Presented) A process according to Claim 25, further comprising annealing the silicon substrate at a temperature below 800°C after forming the drain and

source extensions.

29. (Previously Presented) A process according to Claim 25, wherein implanting the dopants to form the drain and source extensions comprises performing a deep amorphization in the silicon substrate.

30. (Previously Presented) A process according to Claim 29, further comprising recrystallizing the silicon substrate after performing the deep amorphorization.

31. (Previously Presented) A process according to Claim 25, wherein forming the drain and source regions comprises implanting dopants therein.

32. (Previously Presented) A process according to Claim 31, further comprising recrystallizing the silicon substrate after forming the drain and source regions.

33. (Previously Presented) A process according to Claim 27, wherein forming the spacers comprises annealing the silicon substrate at a temperature below 800°C.

34. (Previously Presented) A process according to Claim 27, further comprising annealing the silicon substrate after forming the spacers.

35. (Previously Presented) A process according to Claim 25, further comprising forming pockets in the silicon substrate, the pockets being doped with a dopant having an

opposite conductivity to the dopant implanted when forming the drain and source regions.

36. (Previously Presented) A process according to Claim 35, wherein the pockets are formed before the amorphized regions are formed.

37. (Previously Presented) A process according to Claim 35, wherein the pockets are formed after the amorphized regions are formed.

38. (Previously Presented) A process according to Claim 36, wherein the pockets are formed before the amorphized regions are formed, and before the dopants are implanted in the silicon substrate.

39. (Previously Presented) A process according to Claim 27, wherein the spacers are formed after forming the drain and source extensions.

40. (Previously Presented) A process according to Claim 27, wherein the spacers are formed before the amorphized regions are formed.

41. (Previously Presented) A process according to Claim 25, wherein the amorphized regions have a thickness that is greater than 100 nanometers.

Claim 42 (Cancelled).

43. (Previously Presented) A process according to Claim 25, wherein the source and drain regions are formed by annealing the silicon substrate at a temperature below 800°C.

44. (Previously Presented) A process according to Claim 25, wherein amorphizing the regions of the silicon substrate comprises implanting ions therein.

45. (Previously Presented) A process according to Claim 41, wherein the ions comprise at least one of silicon, germanium, argon, neon, zenon and krypton.

46. (Previously Presented) A process according to Claim 25, wherein the dopants being implanted to form the drain and source extensions comprise at least one of B^+, BF_2^+, In^+, As^+, P^+ and Sb^+.

Claims 47-53 (Cancelled).

54. (Currently Amended) A process for fabricating an integrated circuit comprising:

forming a gate on a silicon substrate;

implanting dopants in the silicon substrate to form drain and source extensions therein;

amorphizing regions of the silicon substrate to obtain amorphous silicon regions adjacent the gate after implanting the dopants; and

~~implanting dopants in the amorphous silicon regions to form drain and source extensions therein; and~~

forming drain and source regions in the respective

drain and source extensions with a channel being defined therebetween, the drain and source regions being formed at a relatively low temperature to avoid diffusion of the dopants from the drain and source extensions.

55. (Previously Presented) A process according to Claim 54, wherein the temperature is within a range of 650 to 800°C.

56. (Previously Presented) A process according to Claim 54, wherein the silicon substrate comprises a crystalline silicon substrate.

57. (Previously Presented) A process according to Claim 54, further comprising forming spacers on the silicon substrate adjacent the gate after forming the drain and source extensions; and annealing the silicon substrate after forming the spacers.

58. (Previously Presented) A process according to Claim 54, wherein implanting the dopants to form the drain and source extensions comprises performing a deep amorphization in the silicon substrate; and further comprising recrystallizing the silicon substrate after performing the deep amorphorization.

59. (Previously Presented) A process according to Claim 54, wherein forming the drain and source regions comprises implanting dopants therein; and further comprising recrystallizing the silicon substrate after forming the drain

and source regions.

60. (Previously Presented) A process according to Claim 54, further comprising forming pockets in the silicon substrate, the pockets being doped with a dopant having an opposite conductivity to the dopant implanted when forming the drain and source regions.

61. (Previously Presented) A process according to Claim 54, wherein the amorphized regions have a thickness that is greater than 100 nanometers.

62. (Previously Presented) A process according to Claim 54, wherein amorphizing the regions of the silicon substrate comprises implanting ions therein.